



Renesas Cuts 66% Off Their 65nm Library Development Schedule

Renesas Addresses Layout Hot Spots Using Takumi Enhance™

Renesas Technology Corp. (Renesas) is one of the top 10 semiconductor suppliers in the world delivering integrated circuits for the fast growing PC/AV, digital consumer and mobile markets. As they decided to move to 65nm process technology, based on their experience with layout hot spots in 90nm cell-based designs, they knew they were up for a stiff challenge.

THE CHALLENGES

- time to market in a tight and unforgiving consumer-driven market
- design-process interactions at sub-wavelength process conditions lead to too many potentially yield-impacting layout hot spots, making manual repair infeasible

THE METHODOLOGY

Renesas, based on their experience with 90nm designs, understood that the number of layout hot spots will be much greater on a 65nm process and that most of them will occur on the critical layers of a dense layout—diffusion, poly and metal1 layers inside cells! Hence, they decided to first address these hot spots on cell “masters” in a library, thereby eliminating the need to fix the same on thousands of cell instances on a completed layout at the RET stage of the design. This provided them with significant savings in effort and time on every sub-wavelength design.

TAKUMI ENHANCE

Takumi Enhance—the automated layout hot spot tool—is designed to detect the most common yield-loss mechanisms (manifesting as layout hot spots) in sub-wavelength designs using foundry and process-specific information. Since not all hot spots are fatal, they are rated for their potential impact to relative yield in terms of parts per billion (PPB). The system using a unique two-dimensional, fully automated lay-

“By working closely with Takumi Technology, we were able to develop a high-yielding 65nm library and significantly reduce the turnaround time. We have now decided to deploy their Takumi Enhance tool in our production flow.”

*Teruaki Harada
Department Manager
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Renesas Technology Corp.*

RENESAS TECHNOLOGY CORP.

- number one supplier of microcontrollers worldwide
- addresses automotive, PC/AV, digital consumer, mobile and industrial markets

DESIGN PROBLEM

- too many layout hot spots to address in 65nm designs
- accelerated time to market

TAKUMI TECHNOLOGY SOLUTION

- implemented a solution using Takumi Enhance, the layout yield optimization platform
- developed Renesas-specific ratings as add-on functions

RESULTS

- reduced risk by increasing hot spot coverage
- slashed two-thirds off the schedule

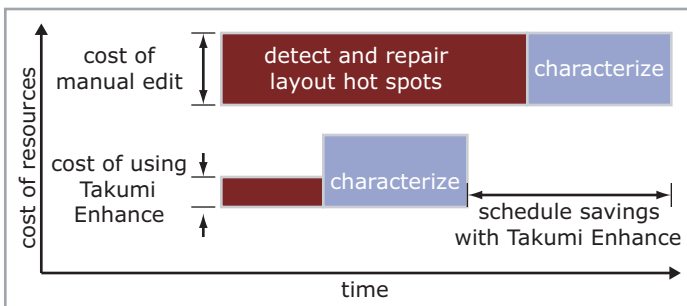
“The automation of fixing hot spots using Takumi’s powerful layout manipulation cut two-thirds off the schedule for our entire library layout team. In addition, the ability to develop and use custom rating functions gave us the yield-enhanced libraries we needed.”

Masayuki Ohayashi
Group Manager
Device IP Development Department
System Solution Business Group
Renesas Technology Corp.

out manipulation technology can optimize the layout taking the relative cost imposed by each of these yield-loss mechanisms.

CUSTOMIZING TAKUMI ENHANCE TO ENSURE COVERAGE OF HOT SPOTS

Failure rates can vary by a lot between similar process nodes in two different fabs or foundries. Hence, the key is to ensure the maximum possible coverage of hot spots. Renesas achieved this by working closely with Takumi Technology Corp. to develop custom rating functions that addressed their foundry and process-specific issues.



ACHIEVING RENESAS OBJECTIVES

The library team achieved their two objectives.

1. *save time and effort*: closure on specific 65nm libraries ended two-thirds ahead of schedule
2. *reduce risk and improve quality*: significantly reduced failure rates in PPB by eliminating hot spots

DEPLOYING TAKUMI ENHANCE INTO PRODUCTION FLOW

After a successful experience, Renesas has now deployed Takumi Enhance for production use.

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