



Takumi Technology Introduces Two New DFM Products for IC Layout Optimization Advanced Tools Detect, Rate and Repair Hot Spots in Sub-90nm Designs

SUNNYVALE, Calif.—July 12, 2006—Takumi Technology Corp., a technology leader in system solutions for design for manufacturing (DFM), today announced two new products designed to optimize IC physical design and enhance yields. Called Takumi Inspect and Takumi Enhance, these new tools detect, rate and automatically repair hot spots in sub-90nm designs.

Takumi Inspect is a layout analysis software tool that detects yield-impacting problems in GDSII layouts that are not detected by DRC or DFM rules and then rates them in terms of their probability of failure. The second tool, Takumi Enhance, is an automated physical design optimization system that rates GDS layouts for potential failures, prioritizes the failure mechanisms, and uses advanced optimization techniques to concurrently repair the layout against multiple failure mechanisms to provide hot spot free designs. Takumi Enhance can also use information generated from other third-party pre- or post-OPC verification tools to drive Takumi's fast 2D layout optimization engine.

Escalating price competition and shrinking market windows are forcing IC designers to ensure that every design works right the first time, so improving design yield and ramp-up time are essential to market success. "While manufacturers have adopted OPC to mitigate sub-wavelength problems in sub-90nm designs, it still does not guarantee hot spot-free designs and high yields," notes Adriaan Ligtenberg, CEO of Takumi Technology. "Working with our technology partners, we've developed two tools that use yield, failure rate, lithography parameters, design rules and other pertinent setup data from the foundries to detect, rate and automatically repair hot spots on a layout without introducing new violations."

Advanced Optimization Techniques

The optimization process begins with Takumi Inspect which analyzes the layout and then, within a single environment, rates potential problems by taking into account a wide range of manufacturing issues that impact yield and robustness including those related to RET/OPC, lithography, random defects, systemic defects, and manufacturing tolerances.

Takumi Enhance operates on GDSII layout data to detect, rate and automatically repair hot spots based on critical area, single contact hole or via, printability and edge placement errors (EPE) due to misalignment margins and contrast issues. In addition, a user can develop a custom criticality rating function using a powerful language-based interface. All of these ratings are performed using foundry-specific defect data.

Key Rating Functions

Critical area analysis (CAA)—The over- or under-correction of a layout by resolution enhancement technology (RET) can cause similar failures in silicon that are similar to the particle defects, which are detected by CAA techniques. Takumi Enhance runs CAA analysis to detect and most importantly rate the defects, especially after OPC.

Single contact hole or via—The single most common robustness improvement technique is to double contacts or vias. Takumi Enhance accomplishes this on an “as needed” as well as “where possible” basis, fully considering the relative priority of the other rating and optimization requirements.

Printability and EPE—The increasing lithography gap forces poor contrast and higher incidence of contact or via cover margin defects in silicon. These result in printability and edge placement errors. Takumi Enhance is designed to detect and repair both types of defects, thereby enhancing yield and turnaround time.

Price and Availability

Pricing starts at \$200,000 depending on the configuration.

Takumi is ready to engage with customers now.

About Takumi Technology Corporation

Founded in October 2003 and headquartered in Sunnyvale, California, Takumi Technology Corp. is the leading provider of design for manufacturing (DFM) systems solutions for sub-wavelength process nodes. Takumi Technology presently offers criticality aware solutions for backend tapeout flow, defect analysis and layout optimization. Takumi’s criticality aware methodologies are completely vendor-agnostic and enable our customers to maximize their productivity and investment in their existing third-party EDA tools. Takumi’s technologies have been deployed with leading IDMs in 90nm, 65nm and 45nm technology nodes. Takumi Technology B.V. (The Netherlands) and Takumi Technology KK (Japan) are wholly-owned subsidiaries of Takumi Technology Corp.

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